4.6 Hardware descripts language and IC technology (ACtE0406)

VHDL Overview

1. What does VHDL stand for?
    - A) Very High Description Language
    - B) Very High-Density Language
    - C) VHSIC Hardware Description Language
    - D) VLSI Hardware Design Language

2. What is the primary use of VHDL?
    - A) Programming microcontrollers
    - B) Designing digital circuits
    - C) Writing software applications
    - D) Simulating analog circuits

3. Which of the following is a key feature of VHDL?
    - A) Object-oriented programming
    - B) Concurrent execution
    - C) Sequential execution only
    - D) None of the above

4. VHDL is primarily used for designing and simulating which type of systems?
    - A) Analog systems
    - B) Digital systems
    - C) Mechanical systems
    - D) Chemical processes

5. Which of the following is a valid data type in VHDL?
    - A) Integer
    - B) Character
    - C) Time
    - D) All of the above

6. Which of the following statements is true about VHDL?
    - A) VHDL is case-sensitive
    - B) VHDL is case-insensitive
    - C) VHDL only supports uppercase keywords
    - D) VHDL only supports lowercase keywords

7. In VHDL, what is the purpose of the "library" keyword?
    - A) To include code from other VHDL files
    - B) To import specific packages
    - C) To define a logic gate
    - D) To declare variables

8. Which VHDL construct is used to model the behaviour of digital circuits?
    - A) Procedure
    - B) Entity
    - C) Process
    - D) Block

9. The entity in VHDL is used to describe:
    - A) Internal signals
    - B) The external interface of a digital component
    - C) The timing constraints
    - D) None of the above

10. Which of the following is true about VHDL signals?
    - A) They are used to store constants
    - B) They are used for inter-process communication
    - C) They cannot be updated
    - D) They are similar to variables in software programming

11. Which of the following describes the behaviour of an entity in VHDL?
    - A) Architecture
    - B) Process
    - C) Function
    - D) Package

12. In VHDL, which construct allows for the definition of reusable blocks of code?
    - A) Package
    - B) Function
    - C) Procedure
    - D) All of the above

13. What does the “architecture” keyword define in a VHDL model?
    - A) A testbench
    - B) The design’s structure or behavior
    - C) Input-output constraints
    - D) A simulation environment

14. In VHDL, what is the role of a "sensitivity list"?
    - A) To list the inputs and outputs
    - B) To specify signals that trigger a process
    - C) To declare variables
    - D) To define timing constraints

15. Which of the following is used to describe the interconnection of components in VHDL?
    - A) Entity
    - B) Architecture
    - C) Configuration
    - D) Signal

<u>Overflow and Data Representation Using VHDL</u>

16. What type of overflow occurs when the result of an arithmetic operation exceeds the range of the data type?
    - A) Sign overflow
    - B) Type overflow
    - C) Arithmetic overflow
    - D) Boolean overflow

17. In a signed number representation in VHDL, what does the most significant bit (MSB) represent?
    - A) The magnitude of the number
    - B) The least significant bit
    - C) The sign of the number
    - D) The overflow indicator

18. Which VHDL construct is used to detect overflow in arithmetic operations?
    - A) Process
    - B) If-Else statement
    - C) Overflow flag
    - D) Signal assignment

19. Which of the following describes two's complement representation?
    - A) It uses a sign bit and magnitude bits
    - B) It represents positive and negative numbers
    - C) It uses an unsigned representation
    - D) It only represents positive numbers

Design of Combinational Logic Using VHDL

20. Which VHDL construct is used to model combinational logic?
    - A) Process with sensitivity list
    - B) Loop statement
    - C) Variable declaration
    - D) Architecture declaration

21. Which of the following can be used to implement a multiplexer in VHDL?
    - A) IF-ELSE statement
    - B) CASE statement
    - C) WHEN-ELSE statement
    - D) All of the above

22. In combinational logic design using VHDL, which construct is often used for priority encoding?
    - A) LOOP
    - B) GENERATE
    - C) IF-ELSE
    - D) PROCEDURE

23. Which of the following is true about combinational circuits?
    - A) They have memory
    - B) They do not have memory
    - C) They always require feedback
    - D) They cannot be implemented using VHDL

24. Which VHDL statement can be used to implement a combinational decoder?
    - A) FOR loop
    - B) CASE statement
    - C) IF-THEN-ELSE statement
    - D) WAIT statement

25. In a combinational logic circuit, the output depends on:
    - A) The present inputs
    - B) The previous state of the system
    - C) The clock signal
    - D) All of the above

26. Which of the following is NOT a combinational logic component?
    - A) Full adder
    - B) Multiplexer
    - C) D flip-flop
    - D) Decoder

27. Which of the following is a combinational circuit that selects one output from many inputs?
    - A) Encoder
    - B) Decoder
    - C) Multiplexer
    - D) Demultiplexer

Design of Sequential Logic Using VHDL

28. In VHDL, sequential logic typically uses:
    - A) Flip-flops
    - B) Multiplexers
    - C) Combinational gates
    - D) Encoders

29. Which VHDL construct is most commonly used to implement sequential logic?
    - A) Process with a clock signal in the sensitivity list
    - B) Concurrent signal assignment
    - C) Case statement
    - D) Entity declaration

30. A D flip-flop can be described in VHDL using:
    - A) A process sensitive to both clock and reset
    - B) A simple signal assignment
    - C) An entity without architecture
    - D) A function call

31. Which of the following can be used to implement a finite state machine (FSM) in VHDL?
    - A) Case statements
    - B) Process with clock and reset signals
    - C) State encoding with ENUM types
    - D) All of the above

32. Sequential circuits differ from combinational circuits because they:
    - A) Have no memory
    - B) Are faster
    - C) Depend on both current inputs and previous states
    - D) Require no clock signals

33. A typical sequential VHDL process uses which two primary signals?

- A) Input and output
- B) Clock and reset
- C) Enable and clock
- D) Data and address

34. Which VHDL statement is used to implement state transitions in a finite state machine (FSM)?
    - A) FOR loop
    - B) CASE statement
    - C) IF-THEN-ELSE
    - D) WAIT statement

35. In VHDL, how can a counter be implemented?
    - A) Using a process triggered by the clock signal
    - B) Using a simple signal assignment
    - C) Using a FOR-GENERATE loop
    - D) Using a function

36. What type of memory element is used in the design of sequential logic?
    - A) Flip-flop
    - B) AND gate
    - C) Multiplexer
    - D) Decoder

37. In VHDL, a process that describes sequential logic should include:
    - A) A clock signal
    - B) Only combinational logic
    - C) A single assignment statement
    - D) A sensitivity list with only input signals

38. Which of the following is an example of sequential logic?
    - A) Full adder
    - B) D flip-flop
    - C) Multiplexer
    - D) Half subtractor

Pipelining Using VHDL

39. Pipelining in digital design helps in:
    - A) Reducing latency
    - B) Increasing throughput
    - C) Minimizing power consumption
    - D) Decreasing the number of clock cycles

40. Which of the following is an essential component of a pipelined design?
    - A) Flip-flop
    - B) Memory element
    - C) Combinational logic
    - D) All of the above

41. In a pipelined design, the clock signal typically:

- A) Only controls the input signals
- B) Synchronizes data transfer between pipeline stages
- C) Controls the output signals directly
- D) Is unnecessary

42. Which of the following best describes the concept of pipelining?
    - A) Dividing a task into stages and processing them in parallel
    - B) Reducing clock frequency
    - C) Using fewer resources for the same task
    - D) All of the above

43. Which of the following best describes the pipeline register?
    - A) It stores intermediate results between pipeline stages
    - B) It delays the clock signal
    - C) It holds the input data for the pipeline
    - D) It manages the control signals of the pipeline

44. In VHDL, pipelining is typically implemented using:
    - A) Multiple clocked processes
    - B) A single combinational process
    - C) An unclocked process
    - D) WAIT statements

45. In a pipelined architecture, what is the role of the control unit?
    - A) To manage data flow between pipeline stages
    - B) To synchronize all pipeline stages
    - C) To detect and handle hazards
    - D) All of the above

46. Pipelining in VHDL can lead to:
    - A) Increased design complexity
    - B) Reduced latency
    - C) Lower power consumption
    - D) None of the above

47. Which of the following is a potential issue in pipelined designs?
    - A) Data hazards
    - B) Pipeline registers
    - C) Control signals
    - D) Reduced clock speed

48. Which of the following hazards can occur in a pipelined system?
    - A) Data hazard
    - B) Control hazard
    - C) Structural hazard
    - D) All of the above

49. In pipelining, a data hazard occurs when:
    - A) Data is not available in time for the next pipeline stage
    - B) The pipeline registers fail
    - C) The clock signal is skewed
    - D) The data does not fit in memory

50. What is a key advantage of using pipelining in digital designs?

- A) Reduced design complexity
- B) Increased clock speed
- C) Higher throughput
- D) Lower latency

51. In pipelining, the control hazard occurs due to:
    - A) Data dependencies
    - B) Incorrect data forwarding
    - C) Branch instructions
    - D) Pipeline register failure

52. What technique can be used to resolve control hazards in a pipeline?
    - A) Branch prediction
    - B) Data forwarding
    - C) Pipeline stalling
    - D) Hazard detection

53. Which of the following is a typical application of pipelining in VHDL?
    - A) Digital filters
    - B) Flip-flop design
    - C) Simple logic gates
    - D) Serial communication protocols

54. In a pipelined system, what does a stall refer to?
    - A) Halting the entire system
    - B) Delaying the pipeline until data becomes available
    - C) Reducing the clock frequency
    - D) Increasing the clock frequency

55. Which of the following is NOT a solution for resolving pipeline hazards?
    - A) Instruction reordering
    - B) Increasing clock speed
    - C) Pipeline interlocks
    - D) All of the above
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56. Pipeline registers are placed:
    - A) At the beginning of the pipeline
    - B) Between each pipeline stage
    - C) At the end of the pipeline
    - D) Only at the input and output stages

57. Which type of pipeline hazard occurs due to resource conflicts?
    - A) Data hazard
    - B) Control hazard
    - C) Structural hazard
    - D) Timing hazard

58. How can structural hazards be avoided in a pipeline?
    - A) By duplicating hardware resources
    - B) By using branch prediction
    - C) By increasing clock speed
    - D) By implementing bypassing techniques

59. Which of the following describes instruction-level parallelism (ILP)?

- A) Executing multiple instructions simultaneously in a pipeline
- B) Executing a single instruction in multiple clock cycles
- C) Delaying instruction execution
- D) Using fewer resources for each instruction

60. A pipeline interlock is used to:
    - A) Detect and prevent hazards in a pipeline
    - B) Speed up the pipeline stages
    - C) Increase the clock frequency
    - D) Reduce the number of pipeline stages

61. In VHDL pipelining, stage balancing refers to:
    - A) Ensuring each pipeline stage has an equal amount of logic
    - B) Doubling the resources of each pipeline stage
    - C) Reducing the clock frequency
    - D) Increasing pipeline depth

62. Which of the following describes the role of the pipeline control unit?
    - A) Managing data dependencies and hazards
    - B) Flushing the pipeline
    - C) Increasing clock speed
    - D) Decreasing power consumption

63. Which of the following is a drawback of pipelining?
    - A) Increased throughput
    - B) Increased complexity of control logic
    - C) Lower power consumption
    - D) Reduced clock frequency