4.3 Input-Output organization and multiprocessor (ACtE0403)

I/O Modules

1. An I/O module serves the primary purpose of:
   - A) Executing instructions
   - B) Connecting peripheral devices to the CPU and memory
   - C) Controlling the speed of the processor
   - D) Managing the operating system

2. Which of the following is NOT a function of an I/O module?
   - A) Data buffering
   - B) Data transmission to peripheral devices
   - C) Executing program instructions
   - D) Error detection and correction

3. Which of these I/O techniques allows the processor to be free for other tasks during data transfer?
   - A) Programmed I/O
   - B) Interrupt-driven I/O
   - C) Direct Memory Access (DMA)
   - D) Polled I/O

4. I/O modules use _____ to notify the processor that an I/O operation has completed.
   - A) Interrupts
   - B) Polling
   - C) DMA
   - D) Cache

5. The I/O control logic that enables communication between the system bus and the peripheral device is called:
   - A) I/O port
   - B) Control register
   - C) Interface unit
   - D) I/O channel

Input-Output Interface

6. An interface between a peripheral device and the computer system is called:
   - A) Gateway
   - B) Bridge
   - C) I/O interface
   - D) Processor register

7. Which of the following I/O interface standards is used for connecting keyboards, mice, and other low-speed peripherals?
   - A) SATA
   - B) PCI Express
   - C) USB
   - D) HDMI

8. The I/O interface used for connecting hard drives and optical drives is:
   - A) PCI
   - B) USB

- C) SATA
- D) HDMI

9. Which interface uses a single data line to transfer data one bit at a time?
    - A) Parallel interface
    - B) Serial interface
    - C) PCI interface
    - D) SCSI interface

Modes of Transfer

10. Which mode of data transfer involves the CPU actively monitoring a peripheral's status until the device is ready to send or receive data?
    - A) Programmed I/O
    - B) Interrupt-driven I/O
    - C) DMA
    - D) Synchronous transfer

11. In which mode of transfer does the CPU get interrupted when the I/O module is ready to transfer data?
    - A) Programmed I/O
    - B) Interrupt-driven I/O
    - C) DMA
    - D) Polled I/O

12. The primary advantage of using DMA for data transfer is:
    - A) It requires fewer CPU cycles
    - B) It transfers data at a faster rate
    - C) It is simpler to implement
    - D) It reduces the amount of memory used

13. Synchronous data transfer mode ensures that:
    - A) Data is transferred one bit at a time
    - B) Data is transferred at a fixed rate
    - C) Data is transferred only when the processor is idle
    - D) Data is transferred simultaneously over multiple channels

14. In which mode of transfer does the CPU continuously check the status of an I/O device?
    - A) Interrupt-driven I/O
    - B) Polled I/O
    - C) Direct Memory Access (DMA)
    - D) Synchronous I/O

15. DMA is typically used for:
    - A) Transferring data between two I/O devices
    - B) High-speed data transfer between I/O devices and memory
    - C) Executing program instructions
    - D) Managing virtual memory

16. Which of the following is NOT a component of the DMA architecture?
    - A) DMA controller
    - B) Memory controller
    - C) System bus
    - D) I/O scheduler

17. When using DMA, the CPU:
    - A) Remains fully engaged in data transfer
    - B) Is relieved of direct control over the data transfer
    - C) Controls the data transfer via interrupts
    - D) Polls the DMA controller continuously

18. In DMA, the process of requesting the use of the bus by the DMA controller is known as:
    - A) Bus Request
    - B) Handshaking
    - C) Bus Grant
    - D) Interrupt signalling

19. The transfer of data from memory to I/O devices using DMA is referred to as:
    - A) Data interrupt
    - B) Block transfer
    - C) Cycle stealing
    - D) Bus mastering

Characteristics of Multiprocessors

20. A multiprocessor system is characterized by:
    - A) Multiple CPUs sharing a common memory
    - B) Multiple CPUs with independent memory
    - C) A single CPU executing multiple threads
    - D) Parallel execution of a single instruction stream

21. Which of the following is an advantage of multiprocessor systems?
    - A) Increased reliability
    - B) Decreased complexity
    - C) Reduced cost
    - D) Easier programming

22. Symmetric multiprocessing (SMP) refers to:
    - A) All processors having equal access to memory and I/O
    - B) One processor controlling all other processors
    - C) Processors having independent memory
    - D) A master-slave configuration

23. In a multiprocessor system, the communication between processors is facilitated by:
    - A) Serial ports
    - B) Shared memory
    - C) Network interfaces
    - D) Interrupt signals

24. A disadvantage of multiprocessor systems is:
    - A) Decreased processing speed
    - B) Increased complexity in synchronization
    - C) Higher power consumption
    - D) Lack of scalability

Interconnection Structure

25. The communication between different components of a computer system is enabled by the:
    - A) CPU
    - B) Memory controller
    - C) Interconnection structure
    - D) Operating system

26. A bus-based interconnection structure typically involves:
    - A) Multiple buses connecting each component to every other component
    - B) A single bus connecting all components to memory and I/O
    - C) A dedicated point-to-point connection between each component
    - D) Processors connected in a circular structure

27. In a crossbar switch interconnection, the primary advantage is:
    - A) Simplicity in design
    - B) Low cost
    - C) High bandwidth between multiple processors and memory modules
    - D) Low latency in communication

28. The primary disadvantage of a fully connected interconnection network is:
    - A) Low bandwidth
    - B) Complexity and high cost
    - C) High latency
    - D) Scalability issues

Inter-processor Communication and Synchronization

29. Inter-processor communication in a multiprocessor system is essential for:
    - A) Parallel execution of independent tasks
    - B) Task synchronization and data sharing
    - C) Reducing processor idle time
    - D) Memory management

30. Which of the following is a common method of inter-processor communication?
    - A) Message passing
    - B) Cache coherence
    - C) Direct Memory Access
    - D) Interrupt handling

31. Cache coherence in multiprocessor systems refers to:
    - A) Ensuring that all caches have the same data at the same time
    - B) Synchronizing the processor clocks
    - C) Reducing memory access time
    - D) Preventing deadlock in memory access

32. Which of the following is a method to achieve synchronization between processors?
    - A) Locks and semaphores
    - B) Virtual memory
    - C) Interrupt-driven I/O
    - D) Direct Memory Access

33. In a shared memory multiprocessor system, race conditions occur when:
    - A) Two processors execute the same program
    - B) Multiple processors attempt to access shared data simultaneously
    - C) One processor has exclusive access to memory
    - D) Processors communicate via message passing

34. Which mode of data transfer is most efficient for bulk data transfer between memory and I/O devices?
    - A) Programmed I/O
    - B) DMA
    - C) Interrupt-driven I/O
    - D) Polling

35. In which type of multiprocessor architecture are all processors connected directly to each other?
    - A) Symmetric multiprocessing
    - B) Clustered multiprocessors
    - C) Tightly coupled multiprocessors
    - D) Loosely coupled multiprocessors

36. Parallel data transfer interfaces are often used for:
    - A) High-speed communication between components
    - B) Reducing power consumption in data transfer
    - C) Single-wire data communication
    - D) Simplifying the design of serial communication systems