Computer Organization and Embedded System

Input-Output Organization and Multiprocessor (ACtE0403)

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4.3 Input-Output Organization and Multiprocessor(ACtE0403):

- Peripheral devices,
- I/O modules,
- Input-output interface,
- Modes of transfer
- Direct Memory access,
- Multiprocessors,
- Interconnection Structure,
- Inter-processor Communication
- Inter-process synchronization

Multiprocessors

- A multiprocessor system is an interconnection of two or more CPUs.
- Can be either a central processing unit (CPU) or an input-output processor (IOP).
- Multiprocessors are classified as Multiple Instruction Stream, multiple Data Stream (MIMD) systems
- Multiprocessor are classified by the way their memory is organized:
  - A multiprocessor system with common shared memory is classified as a shared-memory or **tightly coupled multiprocessor**.
  - Each processor element with its own private local memory is classified as a distributed-memory or **loosely coupled system**.

Interconnection Structures

- The components that form a multiprocessor system are CPUs, IOPs and a Memory Unit.
- The interconnection between the components can have different physical configurations, depending on the **number of transfer paths** that are available:
  - Between the **processors and memory** in a shared memory system
  - Among the **processing elements** in a loosely coupled system

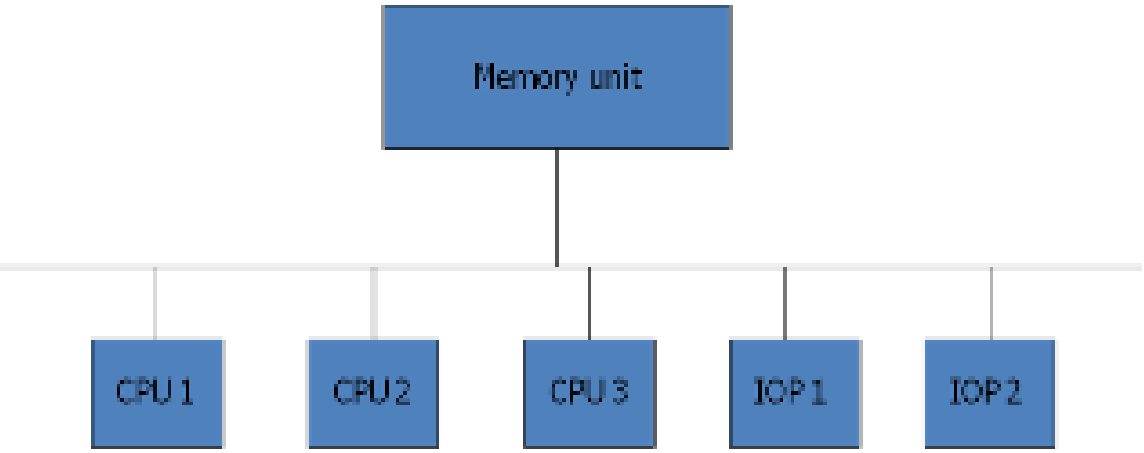
Interconnection Structures

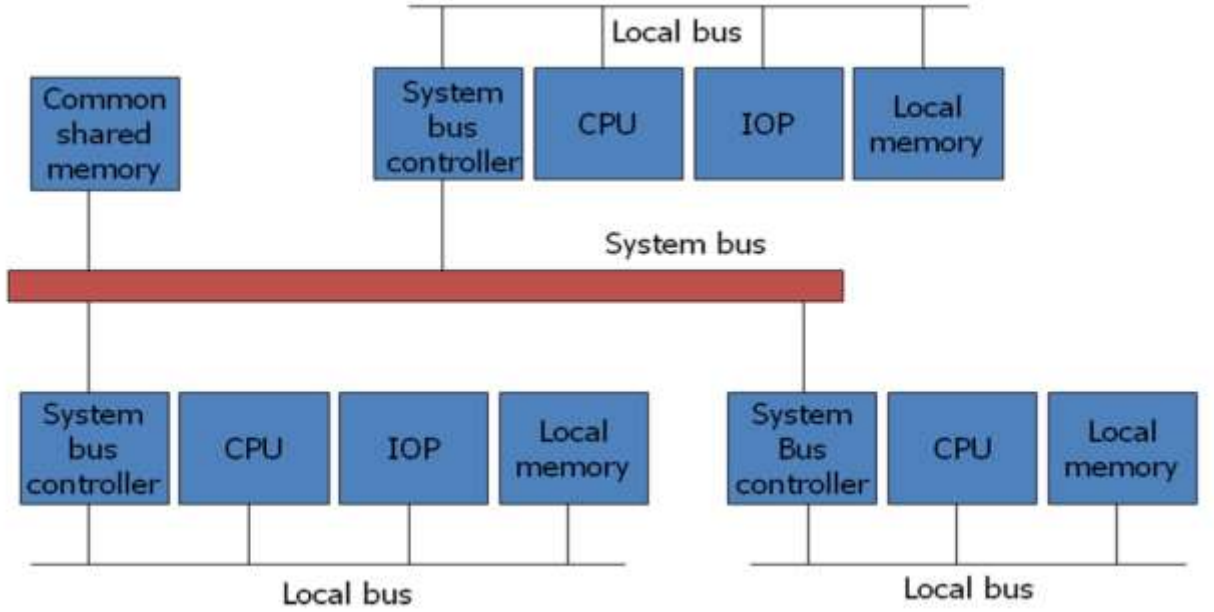
- There are several physical forms available for establishing an interconnection network.
  - Time-shared common bus
  - Multiport memory
  - Crossbar switch
  - Multistage switching network
  - Hypercube system

Time-shared common bus

- A common-bus multiprocessor system consists of a number of processors connected through a **common path to a memory unit**.
- **Disadvantages:**
  - Only one processor can communicate with the memory or another processor at any given time.
  - The total overall transfer rate within the system is limited by the speed of the single path

Time-shared common bus

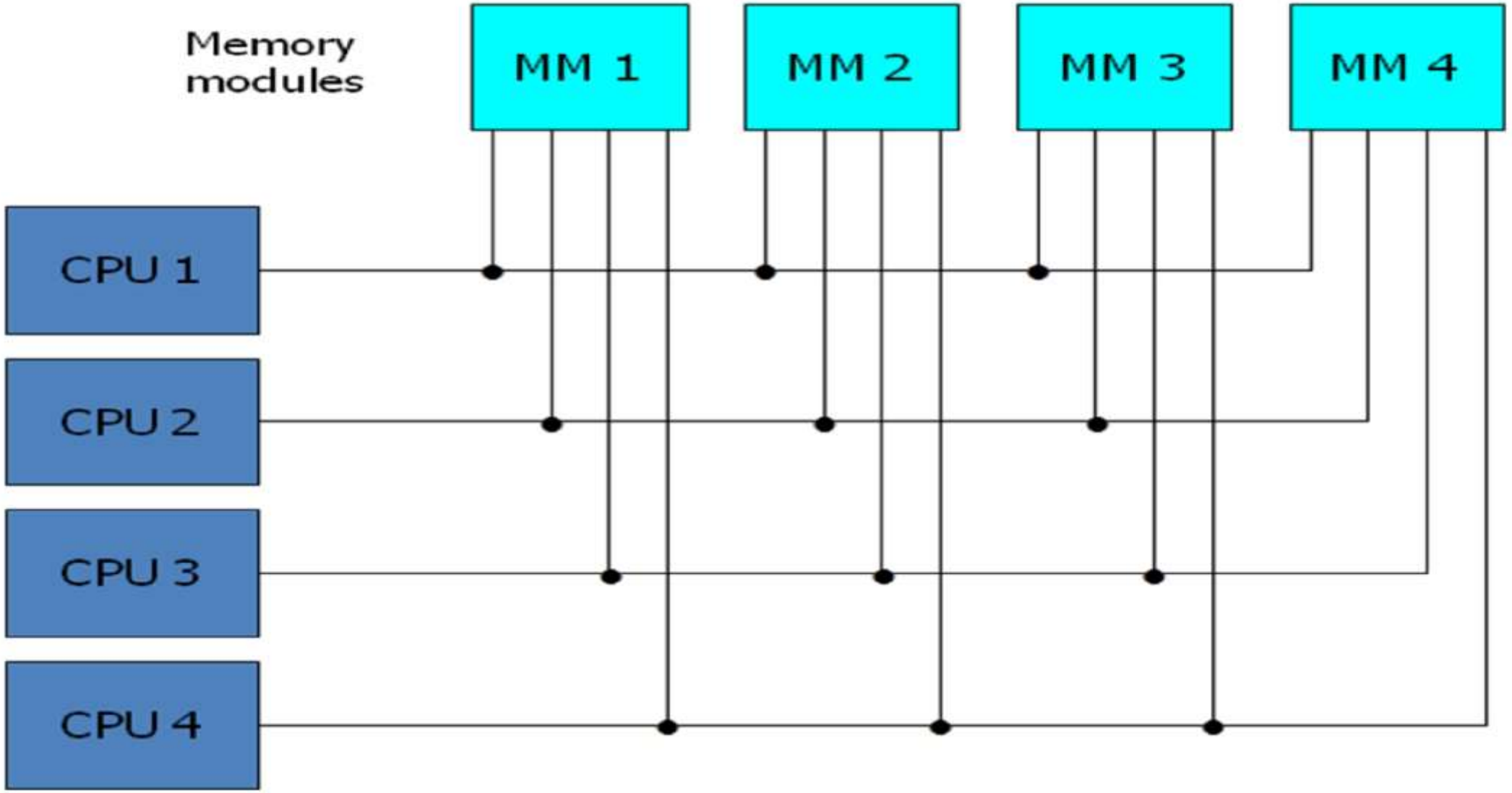




Multiport Memory

- A multiport memory system employs **separate buses** between each memory module and each CPU.
- The module must have **internal control logic** to determine which port will have access to memory at any given time.
- **Advantages:** The high transfer rate can be achieved because of the multiple paths.
- **Disadvantages:** It requires expensive memory control logic and a large number of cables and connections

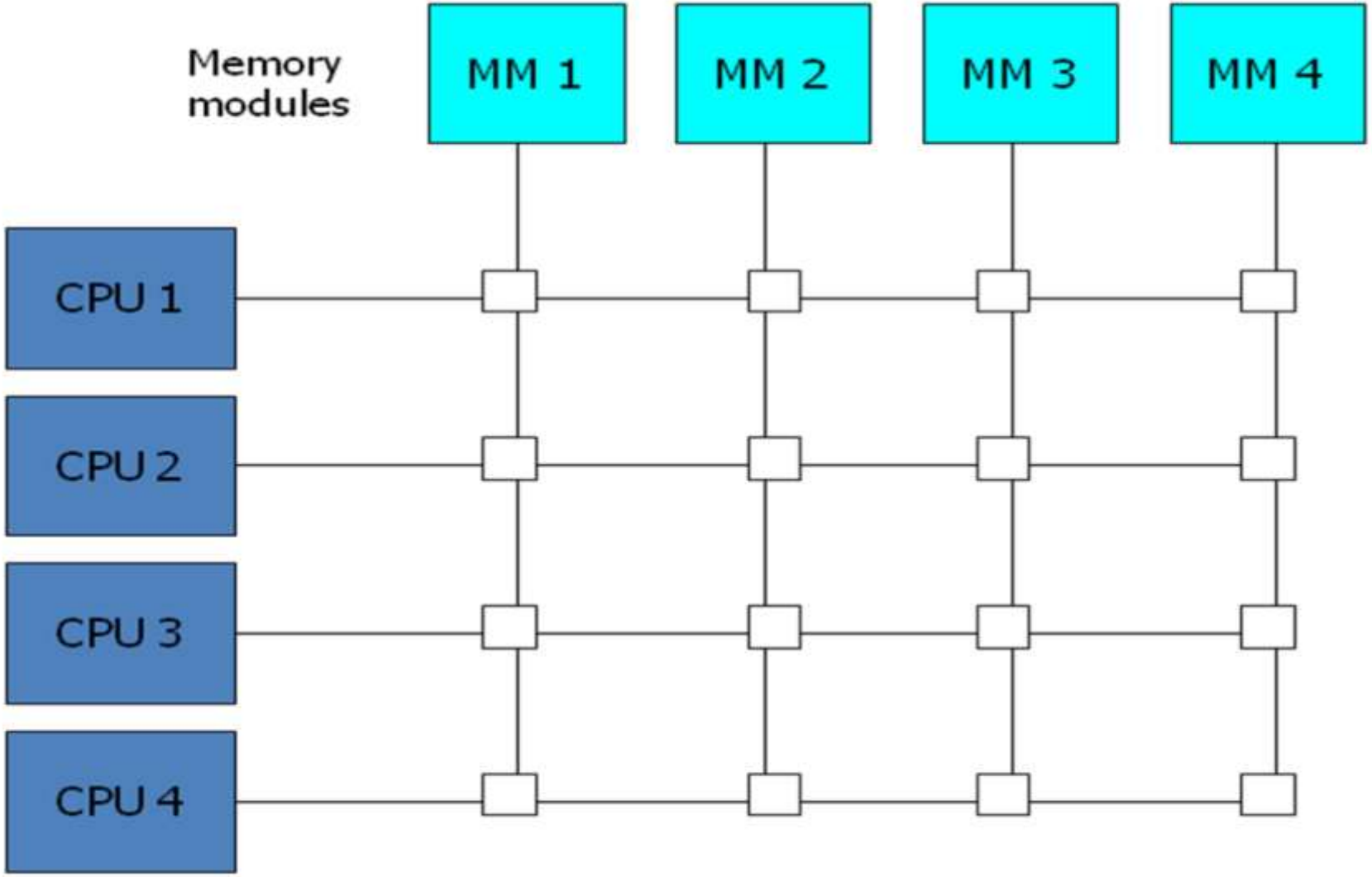
Multiport Memory



Crossbar Switch

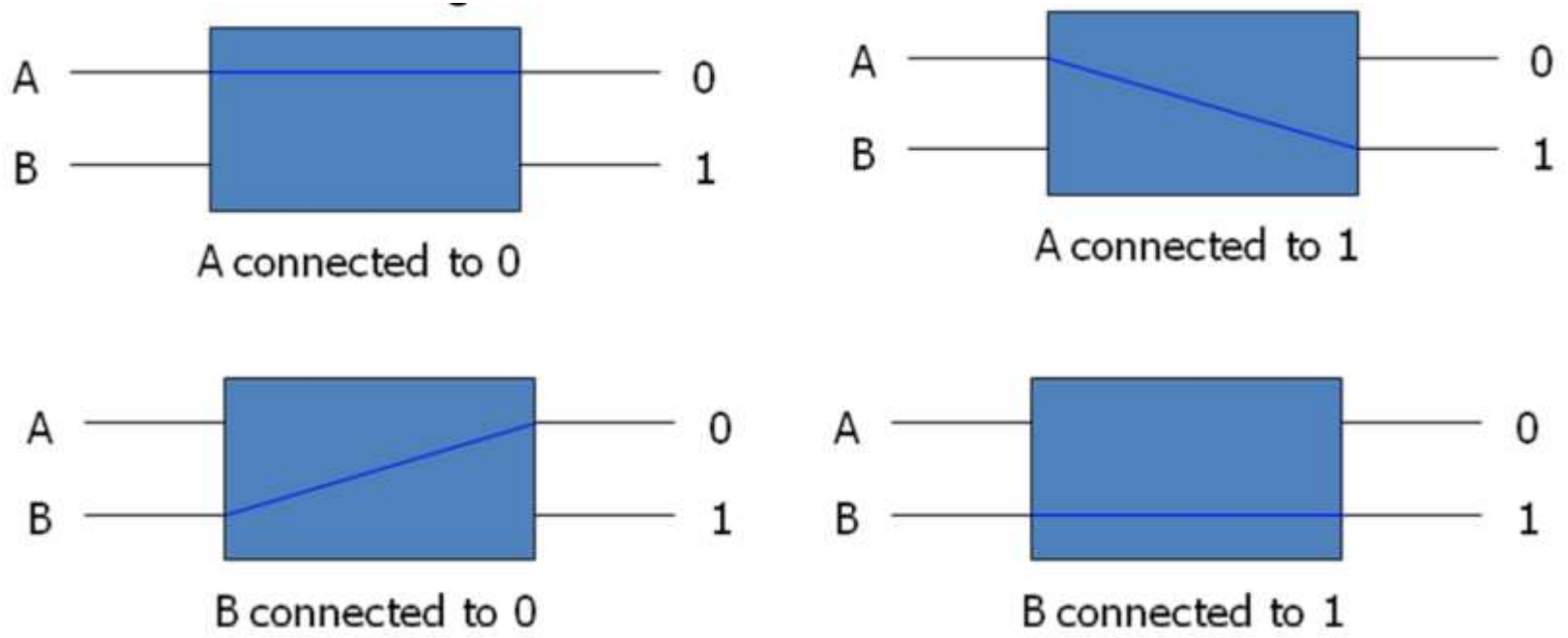
- Consists of a number of **cross-points** that are placed at intersections between processor buses and memory module paths.
- The small square in each cross-point is a switch that determines the path from a processor to a memory module.
- **Advantages:** Supports simultaneous transfers from all memory modules
- **Disadvantages:** The hardware required to implement the switch can become quite large and complex.

Crossbar Switch



Multistage Switching Network

- The basic component of a **multistage network** is a two-input, two-output interchange switch

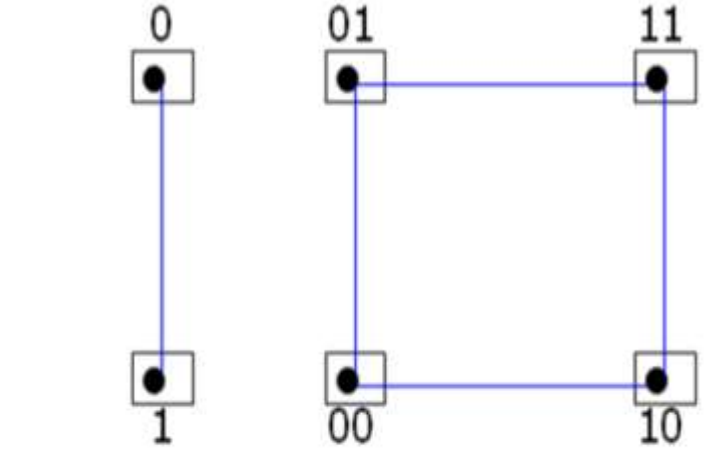


Multistage Switching Network

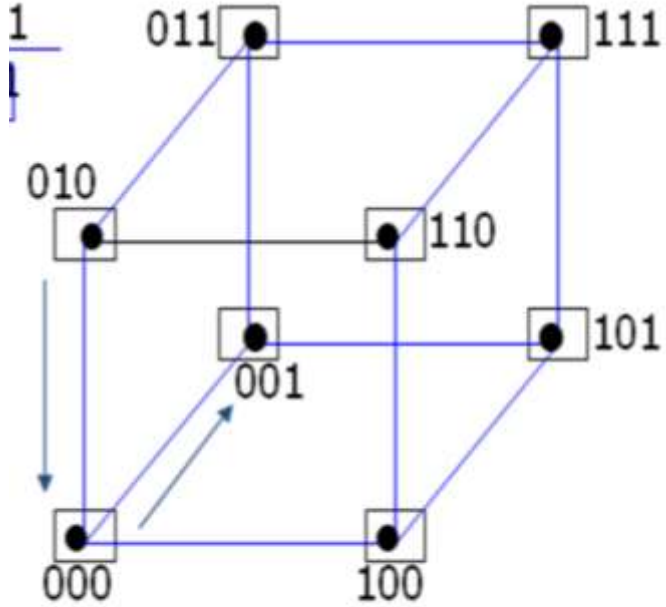
- Some request patterns cannot be connected simultaneously. i.e. any two sources cannot be connected simultaneously to destination.
- In a tightly coupled multiprocessor system, the source is a processor and the destination is a memory module.
  - Set up the path
  - Transfer the address into memory
  - Transfer the data
- In a loosely coupled multiprocessor system, both the source and destination are processing elements.

Hypercube System

- The hypercube multiprocessor structure is a **loosely coupled system** composed of $N=2^n$ processors interconnected in an **n-dimensional binary cube**.
- Each processor **forms** a node of the cube and each processor address differs from that of each of its n neighbours by exactly **one bit position**.
- Routing messages through an n-cube structure may take from one to n links from a source node to a destination node.
- A routing procedure can be developed by computing the **exclusive-OR** of the source node address with the destination node address.



One-cube Two-cube



Three-cube

Inter-processor Communication

- The various processors in a multiprocessor system must be provided with a facility for communicating with each other.
- A communication path can be established through a **portion of memory** or a **common input-output channels**.
- The sending processor structures a **request**, a message, or a procedure, and places it in the **memory mailbox**.
- A more efficient procedure is for the sending processor to alert the receiving processor directly by means of an **interrupt signal**.

Inter-processor Communication

- In **Tightly Coupled System,** the multiprocessor system may have other shared resources. e.g., a magnetic disk storage unit.
- To **prevent conflicting use** of shared resources by several processors there must be a provision for assigning resources to processors. i.e. **operating system**.
- There are three organizations that have been used in the design of operating system for multiprocessors:
  - master-slave configuration,
  - separate operating system,
  - distributed operating system.

Inter-processor Communication

- In a **master-slave mode**, one processor is master and always executes the operating system functions.
- In the **separate operating system** organization, each processor can execute the operating system **routines** it needs.
  - This organization is more suitable for loosely coupled systems.
- In the **distributed operating system** organization, the operating system **routines** are **distributed** among the available processors.
  - Each **particular** operating system function is assigned to only **one processor** at a time.

Inter-processor Communication

- In **Loosely Coupled System**, there is no shared memory for passing information.
- The communication between processors is by means of **message** passing through **I/O channels**.
- The communication is initiated by one processor calling a **procedure** that resides in the **memory** of the **processor** with which it wishes to communicate.
- The communication efficiency of the inter-processor network depends on the **communication routing protocol**, **processor speed**, **data link speed** and the **topology** of the network.

Inter-process Synchronization

- The **instruction set** of a multiprocessor contains basic instructions that are used to implement **communication** and **synchronization** between **cooperating processes**.
- Communication refers to the exchange of **data** between different processes.
- Synchronization refers to the special case where the data used to communicate between processors is **control information**.
- Synchronization is needed to enforce the **correct sequence** of **processes** and to ensure **mutually exclusive access** to shared writable data.

Inter-process Synchronization

- **Mutual exclusion**: This is necessary to **protect data** from being **changed** simultaneously by two or more processors.
- **Critical section**: It is a **program sequence** that must complete execution before another processor accesses the same shared resource.
- A **binary variable** called a **semaphore** is often used to indicate whether or not a processor is executing a critical section.

Thank You.